UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/519,695	03/07/2000	Donglok Kim	OT2.P59	9371

7590 11/18/2002

Koda Law Office
P.O. Box 10057
Bainbridge Island, WA 98110

EXAMINER
LI, AIMEE J

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 11/18/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/519,695	Applicant(s) KIM ET AL.	
	Examiner Aimee J Li	Art Unit 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 March 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☒ Claim(s) *2, 5, and 6* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☒ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

1. Claims 1-21 have been considered.

Oath/Declaration

2. The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

3. The oath or declaration is defective because:

> It does not identify the foreign application for patent or inventor's certificate on which priority is claimed pursuant to 37 CFR 1.55, and any foreign application having a filing date before that of the application on which priority is claimed, by specifying the application number, country, day, month and year of its filing.

Specification

4. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: Figure 8. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Objections

5. Claim 2 is objected to because of the following informalities: Please correct "first cluster of the plurality of clusters and to the first" on page 17, line 20 to read -- first cluster of the plurality of clusters and at the first--. Appropriate correction is required.

6. Claim 5 is objected to because of the following informalities: Please correct "The method of claim 3" on page 18, line 24 to read --The method of claim 4--. Appropriate correction is required.

7. Claim 6 is objected to because of the following informalities: Please correct "moving the compressed instruction into instruction cache" on page 18, line 30 to read -- moving the compressed instruction into an instruction cache --. Appropriate correction is required.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

9. The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

10. Claim 13-16, 19, and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by Pechanek et al., U.S. Patent Number 6,173,389 (herein referred to as Pechanek).

11. Referring to claim 13, Pechanek has taught a computer system comprising:

a. A processor having a very large word instruction architecture and including a plurality of clusters of functional processing units, each one cluster of the

plurality of clusters comprising a common number of functional processing units, the processor comprising a first prescribed number of clusters (Pechanek column 4, lines 42-49; columns 4-5, lines 67-1; column 5, lines 31-32; and Figure 3, elements 101, 151, 196, and 155)

b. Said very large word instruction architecture allowing an instruction to have up to a second prescribed number of subinstructions (Pechanek column 1, lines 39-42 and Figure 2), where the second prescribed number equals the first prescribed number times the common number, each instruction to be executed by the processor comprising from one subinstruction up to the second prescribed number of subinstructions, along with a set of control bits (Pechanek column 4, lines 42-49; columns 4-5, lines 67-1; column 5, lines 31-32; and Figure 3). In regards to Pechanek, the number of clusters is known to determine how many instructions the system is able to process in parallel, and it is inherent that the common number times the first prescribed number equals the second prescribed number because that is the maximum number of instructions that can be processed in parallel.

c. An instructions cache memory (Pechanek column 4, lines 54-56) which stores a first instruction in a compressed format determined by a condition of the set of control bits (Pechanek column 5, lines 61-65), the compressed format including a shared subinstruction stored in a given field of the first instruction which is to be shared by a plurality of the functional processing units (Pechanek column 9, lines 23-25 and Figure 4C), said plurality of functional processing units being

determined by said condition of the set of control bits (Pechanek column 9, lines 28-30 and Figure 4C).

12. Referring to claim 14, Pechanek has taught said shared subinstruction is for a first functional processing unit of a first cluster and a first functional processing unit of a second cluster when the set of control bits identifies a first prescribed condition (Pechanek column 2, lines 24-27; column 10, lines 44-54; and column 11, lines 28-33). In regards to Pechanek, part of the control bits determine whether the instructions being sent are active and need to be loaded and executed by the units.

13. Referring to claim 15, Pechanek has taught shared subinstruction is a first shared subinstruction, and in which the compressed format further includes a second shared subinstruction for a second functional processing unit of the first cluster and a second functional processing unit of the second cluster when the set of control bits either concurrently identifies a second prescribed condition (Pechanek column 10, 44-54).

14. Referring to claim 16, Pechanek has taught:

a. Means for testing the set of control bits for a given instruction (Pechanek column 10, lines 19-22 and 44-54). In regards to Pechanek, the device must test certain control bits in order to determine whether to execute certain types of instructions, and it must also pre-decode the instruction, which identifies the prescribed condition.

b. Means for routing said first common subinstruction to the first functional processing unit of the first cluster and to the first functional processing unit of the second cluster of the plurality of clusters when said testing means identifies the

first prescribed condition (Pechanek column 2, lines 24-27; column 10, lines 44-54; and column 11, lines 28-33).

15. Referring to claim 19, Pechanek has taught:

a. A first instruction in uncompressed format includes the second prescribed number of subinstructions (Pechanek column 1, lines 39-42; column 4, lines 49-50; and Figure 2), the first instruction comprising a first subinstruction for being executed by a first functional processing unit of a first cluster and a second subinstruction for being executed by a first functional processing unit of a second cluster (Pechanek column 2, lines 24-27), the system further comprising means for compressing the first instruction into the compressed format

b. Means for testing the set of control bits associated with the first instruction (Pechanek column 9, lines 6-11). In regards to Pechanek, in order to remove duplicate instructions the control bits must be tested to determine if the instruction has been compressed already.

c. Means for reducing the size of the first instruction by omitting the second subinstruction when the set of control bits identifies that the first subinstruction equals the second subinstruction (Pechanek column 9, lines 6-11).

16. Referring to claim 20, Pechanek has taught:

a. A first instruction in uncompressed format includes the second prescribed number of subinstructions (Pechanek column 1, lines 39-42; column 4, lines 49-50; and Figure 2), the first instruction comprising a first subinstruction for being executed by a first functional processing unit of a first cluster and a second subinstruction

for being executed by a first functional processing unit of a second cluster (Pechanek column 2, lines 24-27), the system further comprising means for compressing the first instruction into the compressed format

b. Means for testing the set of control bits associated with the first instruction (Pechanek column 9, lines 6-11). In regards to Pechanek, in order to remove duplicate instructions the control bits must be tested to determine if the instruction has been compressed already.

c. Means for reducing the size of the first instruction by omitting the second subinstruction when the set of control bits identifies that the first subinstruction equals the second subinstruction (Pechanek column 9, lines 6-11).

d. Means for loading the first instruction into the instruction cache in the compressed format (Pechanek column 4, lines 54-56).

Claim Rejections - 35 USC § 103

17. Claims 1-3 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pechanek et al., U.S. Patent Number 6,173,389 (herein referred to as Pechanek) in view of Dictionary of Computers, Information Processing, and Telecommunications 2nd Edition by Jerry M. Rosenberg © 1987 (herein referred to as Rosenberg).

18. Referring to claim 1, Pechanek has taught a method for sharing a subinstruction of a given instruction among functional processing units of a plurality of clusters on a processor having a very long instruction word architecture (Pechanek column 4, lines 42-49; columns 4-5, clines 67-1; column 5, lines 31-32; and Figure 3, elements 101, 151, 153, and 155), the given instruction including a set of control bits (Pechanek column 6, lines 43-44; column 9, lines 24-

33; and Figure 4C, elements 455) and at least one subinstruction (Pechanek column 1, lines 39-41 and Figure 2), the processor comprising the plurality of clusters, each one cluster of the plurality of the comprising a plurality of functional processing units (Pechanek columns 4-5, lines 67-1; column 2, lines 24-27; and Figure 3). The method comprising the steps of:

a. Testing the set of control bits to identify a prescribed condition (Pechanek column 10, lines 19-22 and 44-54). In regards to Pechanek, the device must test certain control bits in order to determine whether to execute certain types of instructions, and it must also pre-decode the instruction, which identifies the prescribed condition.

b. When the prescribed condition is identified, routing said subinstruction of the given instruction to multiple functional processing units as determined by the prescribed condition (Pechanek column 10, lines 44-54). In regards to Pechanek, part of the control bits determine whether the instructions being sent are active and need to be loaded and executed by the units.

19. Pechanek has not explicitly taught concurrently executing the subinstruction at said multiple functional processing units. However, Pechanek has taught parallel processing in his device (Pechanek column 1, lines 1-18 and 36-37). Rosenberg has taught parallel processing is the concurrent execution of multiple processes in a single unit (Rosenberg page 452, element "parallel processing"). In regards to Rosenberg, Rosenberg has taught that parallel processing inherently means to execute instructions in different processing units and different clusters concurrently. It would have been obvious to a person of ordinary skill in the art to include concurrently executing the subinstructions, because it is inherent in parallel processing.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the concurrent execution of multiple processes taught by Rosenburg in the device of Pechanek.

20. Referring to claim 2, Pechanek has taught routing said subinstruction of the given instruction to a first functional processing unit of a first cluster of the plurality of clusters and to a first functional processing unit of a second cluster of the plurality of clusters (Pechanek column 2, lines 24-27; column 10, lines 44-54; and column 11, lines 28-33).

21. Pechanek has not explicitly taught concurrently executing the subinstruction at said first functional processing unit of the first cluster of the plurality of clusters and to the first functional processing unit of the second cluster of the plurality of clusters. Rosenberg has taught concurrently executing the subinstruction at said first functional processing unit of the first cluster of the plurality of clusters and at the first functional processing unit of the second cluster of the plurality of clusters (Rosenberg page 452, element "parallel processing"). In regards to Rosenberg, Rosenberg has taught that parallel processing inherently means to execute instructions in different processing units and different clusters concurrently. It would have been obvious to a person of ordinary skill in the art to include concurrently executing the subinstructions, because it is inherent in parallel processing. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the concurrent execution of multiple processes taught by Rosenburg in the device of Pechanek.

22. Referring to claim 3, Pechanek has taught a method:

a. In which the given instruction comprises a first subinstruction and a second subinstruction (Pechanek column 1, lines 39-41 and Figure 2).

b. The step of testing comprising testing the set of control bits to identify a first prescribed condition (Pechanek column 10, lines 19-22 and 44-54). In regards to Pechanek, the bits must be tested in order to identify the instruction.

c. The step of routing comprising routing the first subinstruction (Pechanek column 10, lines 44-54). In regards to Pechanek, the first subinstruction must be routed in order to be inputted to the decode and execution unit.

d. Testing the set of control bits to identify a second prescribed condition (Pechanek column 10, lines 19-22 and 44-54). In regards to Pechanek, the bits must be tested in order to identify the instruction.

e. When the second prescribed condition is identified, routing said second subinstruction of the given instruction to a second functional processing unit of the first cluster of the plurality of clusters and to a second functional processing unit of the second cluster of the plurality of clusters (Pechanek column 10, 44-54). In regards to Pechanek, the subinstruction must be routed in order for it to be inputted to another decode and execution unit.

23. Pechanek has not explicitly taught:

a. Concurrently executing the subinstruction at the first functional processing unit and the second functional processing unit

b. Wherein the step of executing comprises concurrently executing the first subinstruction at the first functional processing unit of the cluster, the first subinstruction at the first functional processing unit of the second cluster, the second subinstruction at the second functional processing unit of the first cluster

and the second subinstruction at the second functional processing unit of the second cluster.

24. However, Pechanek has taught a device capable of parallel processing (Pechanek column 1, lines 17-18 and 36-37 and column 11, lines 28-33). Rosenberg has taught:

a. Concurrently executing the subinstruction at the first functional processing unit and the second functional processing unit (Rosenberg page 452, element "parallel processing").

b. Wherein the step of executing comprises concurrently executing the first subinstruction at the first functional processing unit of the cluster, the first subinstruction at the first functional processing unit of the second cluster, the second subinstruction at the second functional processing unit of the first cluster and the second subinstruction at the second functional processing unit of the second cluster (Rosenberg page 452, element "parallel processing").

25. In regards to Rosenberg, Rosenberg has taught that parallel processing inherently means to execute instructions in different processing units and different clusters concurrently. It would have been obvious to a person of ordinary skill in the art to include concurrently executing the subinstructions, because it is inherent in parallel processing. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the concurrent execution of multiple processes taught by Rosenburg in the device of Pechanek.

26. Referring to claim 17, Pechanek has not explicitly taught the first common subinstruction is concurrently executed at the first functional processing unit of the first cluster and the first functional processing unit of the second cluster. However, Pechanek has taught a

device capable of parallel processing (Pechanek column 1, lines 17-18 and 36-37 and column 11, lines 28-33). Rosenberg has taught the first common subinstruction is concurrently executed at the first functional processing unit of the first cluster and the first functional processing unit of the second cluster (Rosenberg page 452, element "parallel processing"). In regards to Rosenberg, Rosenberg has taught that parallel processing inherently means to execute instructions in different processing units and different clusters concurrently. It would have been obvious to a person of ordinary skill in the art to include concurrently executing the subinstructions, because it is inherent in parallel processing. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the concurrent execution of multiple processes taught by Rosenburg in the device of Pechanek.

27. Claims 4-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pechanek et al., U.S. Patent Number 6,173,389 (herein referred to as Pechanek) in view of Tsushima et al., U.S. Patent Number 6,044,450 (herein referred to as Tsushima).

28. Referring to claim 4, Pechanek has taught a method:

a. Wherein each instruction comprises at least one subinstruction and up to a first prescribed number of instructions, the first prescribed number being at least two (Pechanek column 1, lines 39-42 and Figure 2)

b. Wherein the processor is organized into a plurality of clusters equaling a second prescribed number, each one cluster of the plurality of clusters comprising a common number of functional processing units, wherein the common number of functional processing units times the second prescribed number equals the first prescribed number (Pechanek column 4, lines 42-49; columns 4-5, lines 67-1;

column 5, lines 31-32; and Figure 3). In regards to Pechanek, the number of clusters is known to determine how many instructions the system is able to process in parallel, and it is inherent that the common number times the second prescribed number equals the first prescribed number because that is the maximum number of instructions that can be processed in parallel.

c. Wherein for a given instruction having the first prescribed number of subinstructions, each functional processing unit of the plurality of clusters is for executing a respective subinstruction of the given instruction (Pechanek column 9, lines 52-58; Figure 3; and Figure 8).

d. When the pattern is among the set of prescribed patters, setting a set of control bits for the instruction to indicate that said pattern is present (Pechanek column 5, lines 61-65; column 6, lines 32-44; column 9, lines 24-33; and Figure 4C, element 455).

29. Pechanek has not explicitly taught

a. Identifying a pattern in which a subinstruction occurs more than once in the given instruction, said subinstruction being a redundant subinstruction

b. Determining whether the pattern is among a set of prescribed patterns

30. However, Pechanek has taught compressing the instruction (Pechanek columns 8-9, lines 66-1). Tsushima has explicitly taught a compression method:

a. Identifying a pattern in which a subinstruction occurs more than once in the given instruction, said subinstruction being a redundant subinstruction (Tsushima

column 7, lines 58-64). In regards to Tsushima, in order to divide the instruction into groups, a pattern must be indentified in the instruction and more than once.

b. Determining whether the pattern is among a set of prescribed patterns (Tsushima column 7, lines 61-65). In regards to Tsushima, in order to set the group codes, the pattern must be matched with the existing group codes.

31. It would have been obvious to a person of ordinary skill in the art to incorporate the above method of Tsushima, because it is part of a compression method. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the compression method of Tsushima in the device of Pechanek.

32. Referring to claim 5, Pechanek has taught compressing the given instruction when the pattern is among the set of prescribed patterns by deleting one occurrence of the redundant subinstruction in the given instruction to achieve a compressed instruction (Pechanek column 3, lines 54-56).

33. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pechanek in view of Tsushima as applied to claims 4-5 above, and further in view of Dictionary of Computers, Information Processing, and Telecommunications 2nd Edition by Jerry M. Rosenberg © 1987 (herein referred to as Rosenberg). Pechanek has taught:

a. Moving the compressed instruction into an instruction cache (Pechanek column 4, lines 54-56).

b. Testing the set of control bits of the compressed instruction to determing a condition is identified in which subinstruction sharing is to occur for the compressed instruction (Pechanek column 10, lines 44-54).

c. When subinstruction sharing is determined to occur, parsing the compressed instruction to route the redundant subinstruction to a plurality of functional processing units as determined by the identified condition (Pechanek column 2, lines 24-27; column 10, lines 44-54; column 11, lines 28-33; and Figure 3).

34. Pechanek has not explicitly taught concurrently executing the subinstruction at said plurality of functional processing units. (Rosenberg page 452, element "parallel processing"). In regards to Rosenberg, Rosenberg has taught that parallel processing inherently means to execute instructions in different processing units and different clusters concurrently. It would have been obvious to a person of ordinary skill in the art to include concurrently executing the subinstructions, because it is inherent in parallel processing. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the concurrent execution of multiple processes taught by Rosenburg in the device of Pechanek.

35. Claims 7-10, 12, 18, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pechanek et al., U.S. Patent Number 6,173,389 (herein referred to as Pechanek) in view of Colwell et al., U.S. Patent Number 5,057,837 (herein referred to as Colwell).

36. Referring to claim 7, Pechanek has taught a method:

a. Wherein each instruction comprises at least one subinstruction and up to a first prescribed number of instructions, the first prescribed number being at least two (Pechanek column 1, lines 39-42 and Figure 2)

b. Wherein the processor is organized into a plurality of clusters equaling a second prescribed number, each on cluster of the plurality of clusters comprising a common number of functional processing units, wherein the common number of

functional processing units times the second prescribed number equals the first prescribed number (Pechanek column 4, lines 42-49; columns 4-5, lines 67-1; column 5, lines 31-32; and Figure 3). In regards to Pechanek, the number of clusters is known to determine how many instructions the system is able to process in parallel, and it is inherent that the common number times the second prescribed number equals the first prescribed number because that is the maximum number of instructions that can be processed in parallel.

c. Wherein for a given instruction having the first prescribed number of subinstructions, each functional processing unit of the plurality of clusters is for executing a respective subinstruction of the given instruction (Pechanek column 9, lines 52-58; Figure 3; and Figure 8).

d. For a case in which the first subinstruction is the same as the second subinstruction setting a first control bit of a set of control bits associated with the given instruction to a first logic state which indicates that the second subinstruction equals the first subinstruction (Pechanek column 5, lines 61-65).

e. For a case in which the third subinstruction is the same as the fourth subinstruction setting a second control bit of a set of control bits associated with the given instruction to a first logic state which indicates that the fourth subinstruction equals the second subinstruction (Pechanek column 5, lines 61-65).

f. Storing the given instruction with the first control bit and the second control bit (Pechanek column 4, lines 51-56 and Figure 4C).

37. Pechanek has not explicitly taught:

a. For the given instruction, comparing a first subinstruction which is to be processed by a first functional unit of a first cluster of the plurality of clusters with a second subinstruction which is to be processed by a first functional unit of a second luster of a plurality of clusters.

b. For the given instruction, comparing a third subinstruction which is to be processed by a second functional unit of a first cluster of the plurality of clusters with a fourth subinstruction which is to be processed by a second functional unit of a second luster of a plurality of clusters.

38. However, Pechanek has taught the need for shrinking VLIW size (Pechanek column 2, lines 14-18). Colwell has taught how a method of shrinking VLIW size comprising steps:

a. For the given instruction, comparing a first subinstruction which is to be processed by a first functional unit of a first cluster of the plurality of clusters with a second subinstruction which is to be processed by a first functional unit of a second luster of a plurality of clusters (Colwell column 1, lines 32-36 and column 2, lines 26-29). In regards to Colwell, the instructions need to be compared in order to identify which are the same and need to be grouped.

b. For the given instruction, comparing a third subinstruction which is to be processed by a second functional unit of a first cluster of the plurality of clusters with a fourth subinstruction which is to be processed by a second functional unit of a second luster of a plurality of clusters (Colwell column 1, lines 32-36 and column 2, lines 26-29). In regards to Colwell, the instructions need to be compared in order to identify which are the same and need to be grouped.

39. It would have been obvious to a person of ordinary skill in the art to incorporate the VLIW compressions method of Colwell, because Pechanek has mentioned a need to compress VLIW size in his invention. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the VLIW compression of Colwell in the device of Pechanek.

40. Referring to claim 8, Pechanek has taught the step of storing comprises storing the given instruction in an uncompressed format (Pechanek column 4, lines 49-50), and further comprising the steps of compressing the given instruction into a compressed format (Pechanek column 8, line 66), and storing the given instruction in cache in the compressed format (Pechanek column 4, lines 54-56), the step of compressing comprising the steps of:

a. Testing the first control bit associated with the given instruction (Pechanek column 9, lines 6-11). In regards to Pechanek, in order to remove duplicate instructions the control bits must be tested to determine if the instruction has been compressed already.

b. For a case in which the first control bit equals the first logic state compressing the given instruction to reduced size in which one copy of the equal first subinstruction and second subinstruction is omitted to avoid redundant storage of the first subinstruction and the second subinstruction (Pechanek column 9, lines 6-11).

c. Testing the second control bit associated with the given instruction (Pechanek column 9, lines 6-11). In regards to Pechanek, in order to remove duplicate

instructions the control bits must be tested to determine if the instruction has been compressed already.

d. For a case in which the second control bit equals the second logic state compressing the given instruction to reduced size in which one copy of the equal third subinstruction and fourth subinstruction is omitted to avoid redundant storage of the third subinstruction and fourth subinstruction (Pechanek column 9, lines 6-11).

41. Referring to claim 9, Pechanek has taught the step of storing the given instruction in cache in the compressed format (Pechanek column 4, lines 54-56) and further comprising prior to the step of storing, the step of compressing the given instruction into a compressed format (Pechanek column 8, line 66), the step of compressing, comprising the steps of:

a. When the first control bit equals the first logic state compressing the given instruction to reduced size in which one copy of the equal first subinstruction and second subinstruction is omitted to avoid redundant storage of the first subinstruction and the second subinstruction (Pechanek column 9, lines 6-11).

b. When the second control bit equals the second logic state compressing the given instruction to reduced size in which one copy of the equal third subinstruction and fourth subinstruction is omitted to avoid redundant storage of the third subinstruction and fourth subinstruction (Pechanek column 9, lines 6-11).

42. Referring to claim 10, Pechanek has taught the step of storing the given instruction in cache in the compressed format (Pechanek column 4, lines 54-56).

43. Referring to claim 12, Pechanek has taught a method:

a. Wherein each instruction comprises at least one subinstruction and up to a first prescribed number of instructions, the first prescribed number being at least two (Pechanek column 1, lines 39-42 and Figure 2)

b. Wherein the processor is organized into a plurality of clusters equaling a second prescribed number, each one cluster of the plurality of clusters comprising a common number of functional processing units, wherein the common number of functional processing units times the second prescribed number equals the first prescribed number (Pechanek column 4, lines 42-49; columns 4-5, lines 67-1; column 5, lines 31-32; and Figure 3). In regards to Pechanek, the number of clusters is known to determine how many instructions the system is able to process in parallel, and it is inherent that the common number times the second prescribed number equals the first prescribed number because that is the maximum number of instructions that can be processed in parallel.

c. Wherein for a given instruction having the first prescribed number of subinstructions, each functional processing unit of the plurality of clusters is for executing a respective subinstruction of the given instruction (Pechanek column 9, lines 52-58; Figure 3; and Figure 8).

d. For a case in which the first subinstruction is the same as the second subinstruction compressing the given instruction to be stored with the first subinstruction (Pechanek column 9, lines 6-11) and setting a first control bit of a set of control bits associated with the given instruction to a logic state which

indicates that the second subinstruction equals the first subinstruction (Pechanek column 5, lines 61-65).

e. For a case in which the third subinstruction is the same as the fourth subinstruction compressing the given instruction to be stored with the third subinstruction (Pechanek column 9, lines 6-11) setting a second control bit of a set of control bits associated with the given instruction to a logic state which indicates that the fourth subinstruction equals the second subinstruction (Pechanek column 5, lines 61-65).

44. Pechanek has not explicitly taught:

a. For the given instruction, comparing a first subinstruction which is to be processed by a first functional unit of a first cluster of the plurality of clusters with a second subinstruction which is to be processed by a first functional unit of a second luster of a plurality of clusters.

b. For the given instruction, comparing a third subinstruction which is to be processed by a second functional unit of a first cluster of the plurality of clusters with a fourth subinstruction which is to be processed by a second functional unit of a second luster of a plurality of clusters.

c. Storing the given instruction with the first control bit and the second control bit (Pechanek column 4, lines 51-56 and Figure 4C).

45. However, Pechanek has taught the need for shrinking VLIW size (Pechanek column 2, lines 14-18). Colwell has taught how a method of shrinking VLIW size comprising steps:

a. For the given instruction, comparing a first subinstruction which is to be processed by a first functional unit of a first cluster of the plurality of clusters with a second subinstruction which is to be processed by a first functional unit of a second luster of a plurality of clusters (Colwell column 1, lines 32-36 and column 2, lines 26-29). In regards to Colwell, the instructions need to be compared in order to identify which are the same and need to be grouped.

b. For the given instruction, comparing a third subinstruction which is to be processed by a second functional unit of a first cluster of the plurality of clusters with a fourth subinstruction which is to be processed by a second functional unit of a second luster of a plurality of clusters (Colwell column 1, lines 32-36 and column 2, lines 26-29). In regards to Colwell, the instructions need to be compared in order to identify which are the same and need to be grouped.

46. It would have been obvious to a person of ordinary skill in the art to incorporate the VLIW compressions method of Colwell, because Pechanek has mentioned a need to compress VLIW size in his invention. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the VLIW compression of Colwell in the device of Pechanek.

47. Referring to claim 18, Pechanek has taught:

a. The first instruction in an uncompressed format includes the second prescribed number of subinstructions, the first instruction comprising a first subinstruction for being executed by a first functional processing unit of a first cluster and a second subinstruction for being executed by a first functional processing unit of a

second cluster, the system further comprising means for compiling the first instruction (Pechanek column 1, lines 39-42; column 4, lines 42-49; columns 4-5, lines 67-1; column 5, lines 31-32; column 9, lines 52-58; Figure 2; Figure 3; and Figure 8).

b. Means for setting a state of the set of control bits to identify a first prescribed condition when the first subinstruction is equal to the second subinstruction (Pechanek column 5, lines 61-65).

48. Pechanek has not explicitly taught means for comparing the first subinstruction and the second subinstruction. However, Pechanek has taught the need for shrinking VLIW size (Pechanek column 2, lines 14-18). Colwell has taught how a method of shrinking VLIW size comprising means for comparing the first subinstruction and the second subinstruction (Colwell column 1, lines 32-36 and column 2, lines 26-29). In regards to Colwell, the instructions need to be compared in order to identify which are the same and need to be grouped. It would have been obvious to a person of ordinary skill in the art to incorporate the VLIW compressions method of Colwell, which includes means for comparing the first and second subinstructions, because Pechanek has mentioned a need to compress VLIW size in his invention. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the VLIW compression of Colwell in the device of Pechanek.

49. Referring to claim 21, Pechanek has taught:

a. A first instruction in uncompressed format includes the second prescribed number of subinstructions (Pechanek column 1, lines 39-42; column 4, lines 49-50; and Figure 2), the first instruction comprising a first subinstruction for being executed

by a first functional processing unit of a first cluster and a second subinstruction for being executed by a first functional processing unit of a second cluster (Pechanek column 2, lines 24-27), the system further comprising means for caching the first instruction (Pechanek column 4, lines 54-56).

b. Mean for setting a state of the set of control bits associated with the first instruction to identify a first prescribed condition when the first subinstruction is equal to the second subinstruction (Pechanek column 5, lines 61-65).

c. Means for reducing the size of the first instruction to achieve a compressed format by omitting the second subinstruction when the set of control bits identifies that the first subinstruction equals the second subinstruction (Pechanek column 9, lines 6-11).

d. Means for loading the first instruction into the instruction cache in the compressed format Pechanek column 4, lines 54-56).

50. Pechanek has not explicitly taught means for comparing the first subinstruction and the second subinstruction. However, Pechanek has taught the need for shrinking VLIW size (Pechanek column 2, lines 14-18). Colwell has taught how a method of shrinking VLIW size comprising means for comparing the first subinstruction and the second subinstruction (Colwell column 1, lines 32-36 and column 2, lines 26-29). In regards to Colwell, the instructions need to be compared in order to identify which are the same and need to be grouped. It would have been obvious to a person of ordinary skill in the art to incorporate the VLIW compressions method of Colwell, which includes means for comparing the first and second subinstructions, because Pechanek has mentioned a need to compress VLIW size in his invention. Therefore, it would

have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the VLIW compression of Colwell in the device of Pechanek.

51. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Pechanek in view of Colwell as applied to claims 7-10 above, and further in view of Dictionary of Computers, Information Processing, and Telecommunications 2nd Edition by Jerry M. Rosenberg © 1987 (herein referred to as Rosenberg). Pechanek has taught a method comprising the steps of:

a. Storing the given instruction in cache in a compressed format with the first control bit and the second control bit (Pechanek column 4, lines 54-56 and Figure 4C).

b. The compressed format combining the storage of the first subinstruction with the storage of the second subinstruction into a first combined storage when the first control bit is set to the first logic state (Pechanek column 9, lines 6-11 and column 5, lines 61-65)

c. The compressed format combining the storage of the third subinstruction with the storage of the fourth subinstruction into a first combined storage when the second control bit is set to the second logic state (Pechanek column 9, lines 6-11 and column 5, lines 61-65)

d. Testing the first control bit (Pechanek column 9, lines 6-11). In regards to Pechanek, in order to remove duplicate instructions the control bits must be tested to determine if the instruction has been compressed already.

e. When the first control bit is set to the first logic state, routing a content of the first combined storage to the first functional processing unit of the first cluster and the

first functional processing unit of the second cluster (Pechanek column 10, lines 44-54). In regards to Pechanek, the subinstruction must be routed in order to be inputted to the decode and execution unit.

f. When the second control bit is set to the second logic state, routing a content of the second combined storage to the second functional processing unit of the first cluster and the second functional processing unit of the second cluster (Pechanek column 10, lines 44-54). In regards to Pechanek, the subinstruction must be routed in order to be inputted to the decode and execution unit.

52. Pechanek has not explicitly taught:

a. Concurrent execution by the first functional processing unit of the first cluster and the first functional processing unit of the second cluster.

b. Concurrent execution by the second functional processing unit of the first cluster and the second functional processing unit of the second cluster.

53. Rosenberg has taught:

a. Concurrent execution by the first functional processing unit of the first cluster and the first functional processing unit of the second cluster (Rosenberg page 452, element "parallel processing").

b. Concurrent execution by the second functional processing unit of the first cluster and the second functional processing unit of the second cluster (Rosenberg page 452, element "parallel processing").

54. In regards to Rosenberg, Rosenberg has taught that parallel processing inherently means to execute instructions in different processing units and different clusters concurrently. It would

have been obvious to a person of ordinary skill in the art to include concurrently executing the subinstructions, because it is inherent in parallel processing. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the concurrent execution of multiple processes taught by Rosenburg in the device of Pechanek.

Conclusion

55. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

a. Hampapuram et al., U.S. Patent Number 5,787,302, has multiple functional processing units, compression, control bits, parallelism, and instruction caching.

b. Hampapuram et al., U.S. Patent Number 5,878,267, has multiple functional processing units, compression, control bits, parallelism, and instruction caching.

c. Jacobs et al., U.S. Patent Number 5,852,641, has a VLIW processor that processes compressed instructions.

d. Jacobs et al., U.S. Patent Number 5,826,054, has a VLIW processor that uses a compressed instruction format.

56. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (703) 305-7596. The examiner can normally be reached on M-T 7:30am-5:00pm.

57. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

58. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Aimee J. Li
Examiner
Art Unit 2183

November 14, 2002

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100